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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,165	12/18/2001	Franciscus Petrus Widdershoven	NL000722	5094

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,165	WIDDERSHOVEN, FRANCISCUS PETRUS	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed April 24, 2006 in response to PTO Office Action mailed January 23, 2006. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, no claims have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-4 remain pending in this application.

Response to Arguments

3. Applicant's arguments filed April 24, 2006 have been fully considered but they are not persuasive. As to the Remarks, Applicant asserted that the prior art of record does not teach or suggest "identification of a logical series of multiple memory locations".

Examiner respectfully traverses applicant's arguments. Estakhri discloses "selecting a location of a logical series of locations", when Estakhri discloses identifying a current sector of a plurality of sectors and each sector is associated with a range of logical block addresses (see column 18, lines 5-30). Thus, it can be clearly seen that the combination of Rivest and Estakhri discloses the limitation as claimed by applicant.

Rivest teaches a mapping method for serial or parallel transfer that determines whether a current location can be overwritten or rewritten (see column 5, lines 7-35). By constantly keeping a mapping of locations that can be rewritten or overwritten, Rives clearly discloses identifying the locations for writing in advance.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a logical series of multiple memory locations is identified and treated in effect as a single logical memory location) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Although the claims identify a logical series of multiple memory locations, there is no disclosure of treating the logical series of multiple memory locations, in effect, as a single logical memory location.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivest (US 4,691,299) and Sinclair (US 6,069,827) and Estakhri (US 6,772,274).

As in claim 1, Rivest teaches a system comprising:

a memory having locations, each capable of storing a WOM codeword from a WOM code (Fig. 3, element 28; column 3, lines 31-68; column 5, lines 25-28);

a memory selector for selecting a currently selected location of the locations (Fig. 3, elements 22 and 26., column 3, lines 51-58; column 5, lines 23-35); and

a data encoder that encodes a received data value in a new codeword from the WOM code, as a function of the received data value and a previous codeword stored in the currently selected location, the data encoder causing the currently selected location to be changed to a next one in the logical series when the WOM code is exhausted, the data encoder storing the new codeword in the currently selected location (Fig. 3, element 16; column 3, lines 51-58; column 5, lines 7-35).

Rivest does not teach a logical series of the locations as required in claim 1.

Estakhri teaches a flash memory system wherein memory location stores the designation identifying the current sector associated with the predetermined range of logical block addresses corresponding with the memory location (column 18, lines 5-30).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use a logical series of the locations as taught by Estakhri in the system of Rivest because it was well known to reduce inefficiencies associated with keeping track of logical block address to physical block address correlation (column 8, lines 57-60).

Rivest further does not teach a reset circuit that resets the contents of the logical series when the WOM code is exhausted for all locations in the series as required by claim 1.

Sinclair teaches an erasable write-once type memory where the storage locations are arranged as blocks (i.e. logical series of memory locations), and a storage location once written may not be written again before it is erased (i.e. it is exhausted) (Fig. 2; column 5, lines 8-17).

Sinclair further teaches a wear-leveling technique in which a previously exhausted storage location is not reused until all other storage locations are subsequently used, whereupon when all locations in a block are exhausted, the block is erased (Fig. 3; column 6, lines 7-61).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to reset the contents of a logical series of locations

when writing to the locations is exhausted as taught by Sinclair, in the system of Rivest, in accordance with providing wear-leveling as taught by Sinclair, where utilizing an erasable write-once type memory as taught by Sinclair in the system of Rivest would have been obvious due to the similar nature of the problems to be solved, namely to provide write-once non-volatile storage, and also in view of the advantages provided by reusability.

Claim 2 is rejected using the same rationale as for the rejection of claim 2, where it is readily apparent in Rivest that a memory location is exhausted when it contains a second-generation code (Figs. 1 and 2., column 4, lines 16-32), and that unused locations contain an initial codeword (Rivest, column 3, lines 47-51), where it is further apparent that the erasing operation of Sinclair would produce the same initial codeword as in Rivest.

As to claim 3, it is noted that except for the addition of error correction coding (ECC) of the input data word, claim 3 is equivalent to claim 1 for the trivial case of N=1. Furthermore, although the combination of Rivest and Sinclair does not teach applying ECC to the input data words, Examiner takes Official Notice that utilizing ECC in non-volatile storage devices is well known in the art as a means to detect and/or correct errors caused by bit failures. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to encode the data word of Rivest and Sinclair using ECC.

Claim 4 is rejected using the same rationale as for the rejection of claim 1, further noting that Sinclair teaches a plurality of blocks (i.e. a series of logical series) (Fig. 3), both Rivest and Sinclair teach addressable memories (Rivest, column 1, lines 15-32; Sinclair, column 4, lines 45-61), where it is apparent that the series selected for an operation is determined under control of the address.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and

line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

8. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 4, 2006

PIERRE VITAL
PRIMARY EXAMINER